SPECIFICATION

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[METHOD FOR FORMING CONTACT OR VIA PLUG]

Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 91115387, filed July 11, 2002.

Background of Invention

[0001] Field of Invention

[0002] The present invention relates to a method for fabricating a semiconductor device. More particularly, the present invention relates to a method for forming a contact or via plug with small dimensions by using multi-step etching.

[0003] Description of Related Art

[0004] In accompany with the advances of semiconductor technology, semiconductor devices are continuously miniaturized. In order to further increase the device integration in deep sub-micron VLSI techniques, multi-level metal interconnect structures containing more than two metal layers are required. In a multi-level metal interconnect process, two metal layers are electrically connected by via plugs formed in the isolating layer between them, wherein the via plugs are fabricated by forming openings in the isolating layer and filling the openings with metal.

[0005]

In a method for forming a contact or via plug in the prior art, a dielectric layer is formed on a substrate having a first metal interconnect layer thereon. The dielectric layer is patterned to form an opening exposing the first metal interconnect layer, and then the opening is filled with metal to form a metal contact or via plug. Thereafter, a second metal interconnect layer is formed on the substrate contacting with the metal

contact or via plug to electrically connect with the first metal interconnect layer.

[0006] As the integration of integrated circuits (IC) continuously gets higher, the metal interconnects and the metal via plugs are miniaturized correspondingly as well as the devices. However, it is hard to form a contact or via plug having a smaller bottom portion because of the restrictions imposed by lithography process and etching process. Meanwhile, filling metal into an opening having a high aspect ratio is usually a challenge.

Summary of Invention

[0007] Accordingly, this invention provides a method for forming a contact or via plug to break through the restrictions imposed by lithography process and etching process, so as to form a contact or via plug with a smaller bottom portion.

[0008] This invention also provides a method for forming a contact or via plug to solve the problem that a small contact/via hole with a high aspect ratio cannot be easily filled with metal.

[0009]

In a method for forming a contact or via plug of this invention, a dielectric layer is formed on a substrate and then a patterned photoresist layer is formed on the dielectric layer. A portion of the dielectric layer exposed by the photoresist layer is removed to form a first opening with the photoresist layer as a mask. A first liner is then formed on the surfaces of the photoresist layer. The first liner comprises a material such as polymer and is formed with, for example, plasma-enhanced chemical vapor deposition (PECVD). A portion of the dielectric layer under the first opening is removed to form a second opening by using the first liner and the photoresist layer as a mask. The second opening incorporates the first opening, and the etching rate of the first liner is smaller than that of the dielectric layer in the etching process. A second liner is formed on the photoresist layer covering the first liner. The second liner comprises a material such as polymer and is formed with, for example, plasma-enhanced chemical vapor deposition (PECVD). A portion of the dielectric layer under the second opening is removed to form a third opening exposing the substrate by using the second liner and the photoresist layer as a mask. The third opening incorporates the second opening, and the etching rate of the second liner is smaller

than that of the dielectric layer in the etching process. The second liner, the first liner and the photoresist layer are removed and then a conductive material is filled into the third opening to form a contact or via plug. The contact or via plug formed by using the multi-step etching method of this invention has a bottom width smaller than the top width thereof.

[0010] In another method for forming a contact or via plug of this invention, a dielectric layer is formed on a substrate and then a patterned photoresist layer is formed on the dielectric layer. A portion of the dielectric layer exposed by the photoresist layer is removed to form a first opening with the photoresist layer as a mask. Thereafter, the photoresist layer is removed and a first liner is formed on the dielectric layer and in the first opening. The first liner preferably comprises silicon nitride or a metal material. A portion of the dielectric layer under the first opening is removed to form a second opening by using the first liner as a mask. The second opening incorporates the first opening, and the etching rate of the first liner is smaller than that of the dielectric layer in the etching process. Thereafter, a second liner is formed on the substrate covering the first liner. The second liner preferably comprises silicon nitride or a metal material. A portion of the dielectric layer under the second opening is removed to form a third opening exposing the substrate by using the second liner as a mask. The third opening incorporates the second opening, and the etching rate of the second liner is smaller than that of the dielectric layer in the etching process. The second liner and the first liner are removed and then a conductive material is filled into the third opening to form a contact or via plug. The contact or via plug formed by using the multi-step etching method of this invention has a bottom width smaller than the top width thereof. Besides, it is also feasible to directly fill a conductive material into the third opening without removing the first liner and the second liner that comprises silicon nitride or metal. If the first and the second liners comprise silicon nitride, they are taken as a part of the dielectric layer. If the first and the second liners comprise metal, they are taken as a part of the contact or via plug.

[0011] Since a multi-step etching process is used to form a contact/via hole having a smaller bottom portion in the method for forming a contact or via plug of this invention, the restrictions imposed by current lithography and etching processes can be broken through.

[0012] Moreover, the contact/via hole formed by using the method of this invention has a top width larger than the bottom width thereof, so the metal (conductive material) can be easily filled into the contact/via hole.

[0013] Furthermore, since the contact or via plug formed by using the method of this invention has a wider top portion, the resistance of the contact or via plug can be reduced.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0016] FIG. 1A~1G illustrate a process flow of forming a contact or via plug according to a first embodiment of this invention in a cross-sectional view; and

[0017] FIG. 2A~2H illustrate a process flow of forming a contact or via plug according to a second embodiment of this invention in a cross-sectional view.

Detailed Description

[0018] First Embodiment

[0019] FIG. 1A~1G illustrate a process flow of forming a contact or via plug according to the first embodiment of this invention in a cross-sectional view.

[0020] Refer to FIG. 1A, a substrate 100 is provided. A dielectric layer 102, such as a silicon oxide layer, is formed on the substrate 100. A patterned photoresist layer 104 is then formed on the dielectric layer 102.

[0021]

Refer to FIG. 1B, an anisotropic etching process is performed to removed a portion of the exposed dielectric layer 102 to form a first opening 106 with the photoresist

layer 104 as a mask.

[0022] Refer to FIG. 1C, a first liner 108 is formed on the surfaces of the photoresist layer 104 and possibly on the surface of the dielectric layer 102 exposed by the first opening 106. In this embodiment, the first liner 108 comprises a material such as polymer and is formed with, for example, plasma-enhanced chemical vapor deposition (PECVD). The reaction gas used in the PECVD process mainly comprises difluoromethane (CH_2F_2), difluoromethane/octafluorobutene (CH_2F_2/C_4F_8) mixture, or difluoromethane/trifluoromethane (CH_2F_2/CHF_3). The PECVD process is conducted under 1~100 mTorr and with a power of about 500~2000W, a self-bias of approximately 0 ~ 400V and a deposition rate of about 600~6000 Å /min, for example. Moreover, argon (Ar), carbon monoxide (CO), oxygen (O_2) and nitrogen (N_2), etc., can be optionally added into the reaction gas used in the PECVD process.

[0023] Refer to FIG. 1D, an anisotropic etching process is conducted using the first liner 108 and the photoresist layer 104 as a mask to remove a portion of the dielectric layer 102 under the first opening 106 to form a second opening 110. The second opening 110 incorporates the first opening 106, and the etching rate of the first liner 108 is lower than that of the dielectric layer 102 in the etching process. During the anisotropic etching process, the portion of the first liner 108 on the sidewall of the first opening 106 still remains, but the portion at the bottom of the first opening 106 is removed at the beginning of the process. Therefore, the dielectric layer 102 exposed by the first liner 108 and the photoresist layer 104 can be etched to form the second opening 110 that incorporates the first opening 106.

[0024] In this invention, it is noted that the first liner 108 can be formed with a thickness at the bottom of the first opening 106 being smaller than that on the top of the photoresist layer 104, or even approaching to zero, by adjusting the deposition conditions. Thus, when the portion of the first liner 108 at the bottom of the first opening 106 is completely removed, the portion on the top of the photoresist layer 104 still remains and can serve as an etching mask thereafter.

[0025] Refer to FIG. 1E, a second liner 112 is formed on the surfaces of the photoresist layer 104 and the first liner 108, and possibly on the surface of the dielectric layer 102 exposed by the second opening 110. In this embodiment, the second liner 112

comprises a material such as polymer and is formed with PECVD, for example. Since the second liner 112 comprising polymer can be formed with the same method for forming the first liner 108, descriptions of the forming method are omitted.

[0026] Refer to FIG. 1F, an anisotropic etching process is conducted using the second liner 112 and the photoresist layer 104 as a mask to remove a portion of the dielectric layer 102 under the second opening 110 to form a third opening 114 exposing the substrate 100. The third opening 114 incorporates the second opening 110, and the etching rate of the second liner 112 is lower than that of the dielectric layer 102 in the etching process. During the anisotropic etching process, the portion of the second liner 112 on the sidewall of the second opening 110 still remains, but the portion at the bottom of the second opening 110 is removed at the beginning of the etching process. Therefore, the dielectric layer 102 exposed by the second liner 112 and the photoresist layer 104 can be etched to form the third opening 114 that incorporates the second opening 110.

[0027] In this invention, it is noted that the second liner 112 can be formed with a thickness at the bottom of the second opening 110 being smaller than that on the top of the photoresist layer 104, or even approaching to zero, by adjusting the process conditions. Thus, when the portion of the second liner 112 at the bottom of the second opening 110 is completely removed, the portion on the top of the photoresist layer 104 still remains and can serve as an etching mask thereafter.

[0028] Refer to FIG. 1G, the second liner 112, the first liner 108 and the photoresist layer 104 are removed, and then the third opening 114 is filled with an electrically conductive material to form a contact or via plug. The method for filling the third opening 114 comprises, for example, deposit the conductive material all over the substrate 100 and performing etching-back or chemical mechanical polishing (CMP) to remove the conductive material outside the third opening 114.

[0029] In this embodiment, the multi-step etching process is used to form a contact/via hole (the third opening) 114 having a smaller bottom portion, so the restrictions imposed by current lithography and etching processes can be broken through. Moreover, the contact/via hole 114 formed by using the method of this invention has a top width larger than the bottom width thereof, so the conductive material can be

easily filled into the contact/via hole. Furthermore, since the contact or via plug 116 formed by using the method of this invention has a wider top portion, the contact/via resistance can be reduced.

[0030] Second Embodiment

[0031] FIG. 2A~2H illustrate a process flow of forming a contact or via plug according to the second embodiment of this invention in a cross-sectional view.

[0032] Refer to FIG. 2A, a substrate 200 is provided. A dielectric layer 202, such as a silicon oxide layer, is formed on the substrate 200. A patterned photoresist layer 204 is then formed on the dielectric layer 202.

[0033] Refer to FIG. 2B, an anisotropic etching process is performed to removed a portion of the exposed dielectric layer 202 to form a first opening 206 with the photoresist layer 204 as a mask.

[0034] Refer to FIG. 2C, the photoresist layer 204 is removed. A first liner 208 is formed on the dielectric layer 202 and in the first opening 206. In this embodiment, the first liner 208 preferably comprises silicon nitride or a metal material, and can be formed by any known deposition method. It is noted that the first liner 208 can be formed with a thickness at the bottom of the first opening 206 being smaller than that on the top of the dielectric layer 202 by adjusting the deposition conditions.

[0035] Refer to FIG. 2D, an anisotropic etching process is conducted to remove the first liner 208 at the bottom of the first opening 206 and then remove a portion of the exposed dielectric layer 202 to form a second opening 210 with the remaining first liner 208 as a mask. The second opening 210 incorporates the first opening 206, and the etching rate of the first liner 208 is lower than that of the dielectric layer 202 in the etching process. Since the first liner 208 is formed thinner at the bottom of the first opening 206, when the portion of the first liner 208 at the bottom of the first opening 206 is completely removed, the portion remaining on the top of the dielectric layer 202 still remains and can serve as an etching mask thereafter. Meanwhile, the first liner 208 on the sidewall of the first opening 206 remains after the anisotropic etching process.

[0036] Refer to FIG. 2E, a second liner 212 is formed on the dielectric layer 202 and in the second opening 210. In this embodiment, the second liner 212 preferably comprises silicon nitride or a metal material, and can be formed by any known deposition method. It is noted that the second liner 212 can be formed with a thickness at the bottom of the second opening 210 being smaller than that on the top of the dielectric layer 202 by adjusting the deposition conditions.

[0037] Refer to FIG. 2F, an anisotropic etching process is conducted to remove the second liner 212 at the bottom of the second opening 210 and then remove the exposed dielectric layer 202 to form a third opening 214 with the remaining second liner 212 as a mask. The third opening 214 exposes the substrate 200 and incorporates the second opening 210, and the etching rate of the second liner 212 is lower than that of the dielectric layer 202 in the etching process. Since the second liner 212 is formed thinner at the bottom of the second opening 210, when the portion of the second liner 212 at the bottom of the second opening 210 is removed, the portion on the top of the dielectric layer 202 still remains. The second liner 212 remaining on the top of the dielectric layer 202 can serve as an etching mask for forming the third opening 214. Meanwhile, the second liner 212 on the sidewall of the second opening 210 remains after the anisotropic etching process.

[0038] Refer to FIG. 2G, a conductive material is directly filled into the third opening 214 to form a contact or via plug 216. The method for filling the third opening 214 comprises, for example, depositing the conductive material all over the substrate 200 and performing etching-back or chemical mechanical polishing (CMP) to remove the conductive material outside the third opening 214. In this embodiment, the contact or via plug is formed without removing the first liner 208 and the second liner 212 previously because the first liner 208 and the second liner 212 comprise metal or silicon nitride. If the first and the second liners 208 and 212 comprise metal, they are taken as a part of the contact or via plug 216; if the first and the second liners 208 and 212 comprise silicon nitride, they can serve as an insulating layer.

[0039] Nevertheless, in this embodiment, the contact or via plug can alternatively be formed by filling the conductive material into the third opening 214 after the first liner 208 and the second liner 212 are removed.

[0040] In this embodiment, the multi-step etching process is used to form a contact/via hole 214 having a small bottom portion, so the restrictions imposed by current lithography and etching processes can be broken through. Moreover, the contact/via hole 214 formed by using the method of this invention has a top width larger than the bottom width thereof, and the conductive material can be easily filled into the contact/via hole 214. Furthermore, since the contact or via plug 216 formed by using the method of this invention has a wider top portion, the contact/via resistance can be reduced.

[0041] The contact/via holes are formed with three-step etching in the first and the second embodiments of this invention, however, the methods for forming a contact/via hole is not only restricted to three-step etching, but also include two-step etching and the etching methods comprising more than three etching steps.

[0042] As mentioned above, since a multi-step etching process is used to form a contact/via hole having a small bottom portion in the method for forming a contact or via plug of this invention, the restrictions imposed by current lithography and etching processes can be broken through. Moreover, the contact/via hole formed by using the method of this invention has a top width larger than the bottom width thereof, and the metal (conductive material) can be easily filled into the contact/via hole. Furthermore, since the contact or via plug formed by using the method of this invention has a wider top portion, the contact/via resistance can be reduced.

[0043] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.